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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,736	01/23/2002	Satoshi Ikeda	SON-2313	3283

23353 7590 06/02/2004

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/052,736	IKEDA, SATOSHI
	Examiner	Art Unit
	James C Kerveros	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *1-3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it fails to comply with the proper language and format for an abstract of the disclosure.

On line 1, the term "Disclosed" should be deleted. Also, the term "means" recited on lines 5, 10, 11, 12 should be avoided. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Correction is required. See MPEP § 608.01(b).

2. The specification is objected to under 37 CFR 1.71 because the specification lacks an enabling description for claims 1-5, in reference to the limitation "the set information" recited in the independent claims 1 and 4.

Claim Objections

3. Claims 1-3 are objected to because of the following informalities:

Claim 1, the term "any address" should be changed to "an address" due to a typo error. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-5 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification lacks enabling description with respect to claimed limitation of "the set information" recited in the independent claims 1 and 4.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 5 recite the limitation "the set information", which lacks antecedent basis. Also, the term " the set information " in claims 1 and 5 is a relative term, which renders the claim indefinite. The term "the set information" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The claimed limitation of "outputting the test pattern of a desired address at a

predetermined timing" has been rendered indefinite, by the use of "the set information", since there is no clear linkage between the two limitations.

Regarding claims 1 and 3, the phrase "such a manner" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Kurosaki (US 6314536).

Regarding independent Claims 1 and 4, Kurosaki discloses a semiconductor memory testing apparatus and method (1, FIG. 1), wherein a test signal (test pattern signal) S1 is supplied to an IC memory under test (3) and a read-out signal S3 is compared with an expected value pattern signal S2 supplied from the pattern generator 2 in the logical comparator 4, said apparatus comprising:

A pattern generator 2, which includes test pattern memory means for storing test pattern data (expected value pattern signal) S2 and outputting S2 to the logical comparator as specified by an address signal (AD) from the pattern generator.

Also, the pattern generator 2 includes test pattern generation means for generating a test pattern signal S1 on the basis of the (expected value pattern signal) S2 from the test pattern memory means.

Control means (system controller 6) for controlling the test pattern memory means (S2) and the test pattern generation means (S1) in the pattern generator 2, that the pattern generating program stored in the system controller (6) is created, such that the pattern generator 2 generates, in addition to address signals which is supplied to the memory under test 3, address signals to be supplied to the failure analysis memory 5, at a predetermined timing using the controlling circuit 8, in accordance with the pattern generating program.

Regarding Claims 2 and 3, Kurosaki discloses control means (system controller 6), which controls the timing of generation of the test pattern and varies the cycle period to execute the test pattern of the desired address. The system controller 6 varies the cycle period by controlling circuit 8 which is capable of producing two burst address signals in one test period at twice the pulse repetition rate of the test period signal TI. The controller includes a multiplexer 12 which selects address signal AD at terminal "a" from the pattern generator 2 or the burst address signal at the terminal "b" from the adder 11 and outputs the selected address signal at terminal "c", which is supplied to the address terminal "A" of the failure analysis memory 5 and the memory under test 3.

Note that the address signal supplied to the MUT 3 on reading the stored test pattern signal out of the MUT 3 is also supplied to the failure analysis memory 5. Timing diagram, FIG. 2A, shows the first address (ADR0) corresponding to address signal (AD) and FIG. 2C shows the burst address signals produced internally of the memory under test 3, respectively. The cycle period of FIG. 2C is double the period of FIG. 2A.

Regarding Claim 5, Kurosaki discloses supplying the input signal of the test pattern (S1) to the semiconductor device MUT 3 after varying the desired address (AD) and the predetermined timing, and detecting whether any failure has been caused or not in the semiconductor device, by comparing the read-out signal S3 from the MTU 3 with an expected value pattern signal S2 in the logical comparator 4. A failure signal FD of logic "1" is outputted from the logical comparator 4 to memory 5 in which failure data corresponding to the failure signal FD is stored at an address of the failure analysis memory 5 specified by an address signal supplied to its address terminal "A". After the completion of the tests, the failure data stored in the failure analysis memory 5 are read out, and a failure analysis of the MUT 3 is performed.

Conclusion

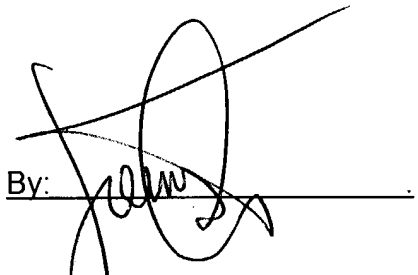
7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

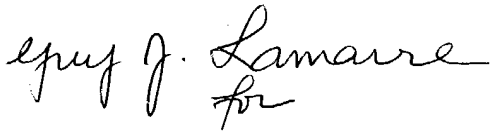
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 24 May 2004
Office Action: Non-Final Rejection

By: 

James C Kerveros
Examiner
Art Unit 2133



Albert DeCady
Primary Examiner